REMARKS[1]

In the outstanding Office Action, the Examiner rejected claims 1-17 under 35 U.S.C. § 102(b) as being anticipated by Japanese Patent Publication No. 05-029533 to Takashi ("Takashi"). Claims 1-31 remain pending in this application, of which claims 1-17 are currently presented for examination.

Applicant gratefully acknowledges the Examiner's withdrawal of the final rejection of claims 1-17, as previously set forth in the final Office Action mailed April 5, 2006, which was replaced with the non-final Office Action mailed June 22, 2006, to which Applicant now responds.

Regarding the Examiner's rejection of claims 1-17 under 35 U.S.C. § 102(b), Applicant respectfully disagrees with the Examiner's assertions and conclusions as set forth in the Office Action. Accordingly, Applicant respectfully traverses this rejection.

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference ... [t]he identical invention must be shown in as complete detail as is contained in the . . . claim." M.P.E.P. § 2131 8th Ed. (Rev. 4), October, 2005 (internal citations omitted).

Takashi cannot anticipate independent claims 1 and 6 because Takashi fails to teach a combination including at least "a plurality of chip interconnections ... formed into substantially the same pattern," and "a plurality of intermediate interconnections ... formed into a pattern different from the pattern of the chip interconnections," as recited in claims 1 and 6 (emphasis added). Takashi shows in Figures 1(a)-1(b) and 2(e)-2(g),

[1] The Office Action contains a number of statements reflecting characterizations of the related art and the claims. Regardless of whether any such statement is identified herein, Applicant declines to automatically subscribe to any statement of characterization in the Office Action.

for example, chips 3a-3n mounted on chip mounting boards, wherein the chips 3a-3n and mounting boards are stacked in a structure having an intermediate layer 7b therebetween. However, Takashi does not teach that chip interconnections connected to chips 3a-3n are "formed into substantially the same pattern," as recited in claims 1 and 6.

Moreover, to the extent that intermediate layer 7b could be reasonably construed as constituting Applicants' claimed "interconnection base," Takashi fails to show any intermediate interconnections connected to chip interconnections "formed into a pattern different from the pattern of the chip interconnections," as also recited in claims 1 and 6.

Because Takashi fails to teach each and every element recited in claims 1 and 6, claims 1 and 6 are allowable over Takashi. Moreover, claims 2-5 and 7-11 are allowable at least due to their respective dependence on claims 1 and 6.

Claim 12, although of different scope, recites elements similar to those recited in claims 1 and 6. Accordingly, claim 12 is allowable over Takashi for at least the reasons given above with respect to claims 1 and 6. Furthermore, claims 13-17 are allowable at least due to their dependence from claim 12.

Takashi also fails to teach a combination including "chip mounting bases," and "interconnection bases," as also recited in claims 1, 6, and 12 (emphasis added). That is, Takashi fails to teach a device having two different types of bases, one of which wherein semiconductor chips are mounted on and an interconnection wherein base semiconductor chips are not mounted on. Takashi, by contrast, teaches only one kind of base. The Examiner asserts, however, that Takashi teaches "one interconnection base which is interposed between two chip (3a-3n) mounting bases (1a-1n, 23a-23n)."

Applicant notes that Takashi at, for example, paragraphs [0013]-[0016], [0027]-[0029], and FIGS. 1 (a)-(d) and 4 (a)-(d), teaches the use of only one type of base.

Applicant notes that Takashi specifically teaches that semiconductor chips (3a-3n) are mounted on bases (1a-1n, 23a-23n). Then, substrates (31a-31n, 33a-33n) are formed by arranging insulator layers (4a-4n, 24a-24n) on the bases (1a-1n, 23a-23n) on which semiconductor chips are mounted. Circuit forming substrates (32a-32n, 34a-34n) are formed by arranging wiring layers (5a-5n, 27a-27n) on the substrates (31a-31n, 33a-33n). Accordingly, the bases (1a-1n, 23a-23n), the substrates (31a-31n, 33a-33n) and the circuit forming substrates (32a-32n, 34a-34n) are substantially the same members. Takashi thus teaches that semiconductor chips (3a-3n) are mounted on all of the bases (1a-1n, 23a-23n), the substrates (31a-31n, 33a-33n) and the circuit forming substrates (32a-32n, 34a-34n). Takashi thus cannot provide a teaching of "chip mounting bases," and "interconnection bases," as recited in claims 1, 6, and 12.

Applicant further notes that because Takashi does teach using different kinds of bases, i.e., "chip mounting bases," and "interconnection bases," as recited in claims 1, 6, and 12, Takashi also cannot teach at least "intermediate interconnections electrically connected to the chip interconnections," as recited in claims 1, 6 and 12 of the present application. Accordingly, claims 1, 6, and 12 are allowable over Takashi for these additional reasons, and claims 2-5, 7-11, and 13-17 are allowable at least because of their dependence from claims 1, 6, and 12. Accordingly, Applicant respectfully requests that the Examiner withdraw the rejection of claims 1-17 under 35 U.S.C. § 102(b).

In view of the foregoing and remarks, Applicant respectfully requests reconsideration and reexamination of this application and the timely allowance of the pending claims.

Please grant any extensions of time required to enter this response and charge any additional required fees to our deposit account 06-0916.

Respectfully submitted,

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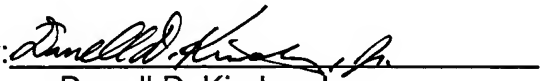
By: 
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